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Claims

[c1] 1. A method of fabricating a semiconductor device, comprising the steps of:
providing a substrate having a first region and a second region;
forming a plurality of stack gate structures on the first region and the second region of the substrate, wherein each stack gate structure comprises a gate dielectric layer a gate dielectric layer next to the substrate, a gate conductive layer in the middle and a cap layer on top;
forming a spacer on each side of the stack gate structure;
forming a plurality of conductive regions in the substrate between the stack gate structures;
forming a first dielectric layer over the substrate, wherein the top surface of the first dielectric layer exposes the cap layers;
forming a buffer layer over the substrate within the first region to cover the first dielectric layer and the cap layers;
removing a portion of the cap layers of the stack gate structure within the second region so that the cap layers within the second region have a thickness smaller than

or equal to the buffer layer;

forming a second dielectric layer over the first region and the second region of the substrate;

forming a first mask layer over the second dielectric layer, wherein the first mask layer having:

a plurality of first openings within the first region formed above various conductive regions; and

a plurality of second openings with the second region formed above various cap layers of the stack gate structures;

removing the second dielectric layer and its underlying buffer layer as well as cap layers within the first opening and the first dielectric layer within the second openings to form a plurality of first contact openings and a plurality of second contact openings respectively, wherein the first contact openings expose various conductive regions within the first region and the second contact openings expose various gate conductive layers of the stack gate structures within the second region; and

removing the first mask layer.

[c2] 2. The method of claim 1, wherein the buffer layer and the cap layer are fabricated using an identical material, and furthermore, has an etching rate different from the second dielectric layer and the first dielectric layer.

[c3] 3. The method of claim 2, wherein the step of forming the first contact openings and the second contact openings further comprises:
performing a first etching operation to remove the second dielectric layer within the first openings and the second openings so that the first openings expose the buffer layer and the second openings expose the cap layers;
performing a second etching operation to remove the buffer layer within the first opening and the cap layer within the second openings so that the first openings expose the first dielectric layer and the second openings expose the gate conductive layer of the stack gate structures in the second region to form the second contact openings; and
performing a third etching operation to remove the first dielectric layer within the first openings to form the first contact openings.

[c4] 4. The method of claim 3, wherein the first etching operation, the second etching operation and the third etching operation are all carried out inside the reaction chamber of a processing station.

[c5] 5. The method of claim 4, wherein material constituting the buffer layer and the cap layer comprises silicon nitride formed using gaseous reactants CF_4, CHF_3, O_2 and

Ar.

[c6] 6. The method of claim 2, wherein the first mask layer further comprises a plurality of third openings within the second region above some of the conductive regions, and the step of removing the second dielectric layer and its underlying buffer layer and cap layer within the first openings and the first dielectric layer within the second openings comprises:
removing the second dielectric layer and its underlying first dielectric layer within the third openings to form the third contact openings.

[c7] 7. The method of claim 6, wherein the step of forming the first contact openings, the second contact openings and the third contact openings further comprises:
performing a first etching operation to remove the second dielectric layer within the first openings, the second openings and the third openings so that the first openings expose the buffer layer, the second openings expose the cap layer and the third openings expose the first dielectric layer;
performing a second etching operation to remove the buffer layer within the first openings and the cap layer within the second openings so that the first openings expose the first dielectric layer and the second openings expose the gate conductive layer of the stack gate struc-

tures in the second region to form the second contact openings; and

performing a third etching operation to remove the first dielectric layer within the first openings and the third openings to form the second contact openings and the third contact openings.

[c8] 8. The method of claim 7, wherein the first etching operation, the second etching operation and the third etching operation are all carried out within the reaction chamber of a processing station.

[c9] 9. The method of claim 8, wherein material constituting the buffer layer and the cap layers comprises silicon nitride formed using gaseous reactants CH_4, CHF_3, O_2 and Ar.

[c10] 10. The method of claim 2, wherein the step of forming the buffer layer over the first region of the substrate and removing a portion of the cap layer of the stack gate structures in the second region further comprises:

forming a buffer material layer over the substrate to cover the first dielectric layer and the cap layers;

forming a second mask layer over the material buffer layer within the first region so that the buffer material layer in the second region is exposed; and

removing the buffer material layer in the second region

and removing a portion of the cap layers of the stack gate structures in the second region so that the remaining cap layers in the second region have a thickness smaller than or equal to the buffer material layer.

[c11] 11. A method of fabricating a semiconductor device, comprising the steps of:
providing a substrate having a first region and a second region;
forming a plurality of stack gate structures on the first region and the second region of the substrate, wherein each stack gate structure comprises a gate dielectric layer a gate dielectric layer next to the substrate, a gate conductive layer in the middle and a cap layer on top;
forming a spacer on each side of the stack gate structure;
forming a plurality of conductive regions in the substrate between the stack gate structures;
forming a first dielectric layer over the substrate, wherein the top surface of the first dielectric layer exposes the cap layers;
forming a buffer layer over the substrate within the first region to cover the first dielectric layer and the cap layers, wherein the buffer layer has a thickness greater than or equal to the cap layers;
forming a second dielectric layer over the first region

and the second region of the substrate;
forming a first mask layer over the second dielectric layer, wherein the first mask layer having:
a plurality of first openings within the first region formed above various conductive regions; and
a plurality of second openings with the second region formed above various cap layers of the stack gate structures;
removing the second dielectric layer and its underlying buffer layer as well as cap layers within the first opening and the first dielectric layer within the second openings to form a plurality of first contact openings and a plurality of second contact openings respectively, wherein the first contact openings expose various conductive regions within first region and the second contact openings expose various gate conductive layers of the stack gate structures; and
removing the first mask layer.

[c12] 12. The method of claim 11, wherein the buffer layer and the cap layer are fabricated using an identical material, and furthermore, has an etching rate different from the second dielectric layer and the first dielectric layer.

[c13] 13. The method of claim 12, wherein the step of forming the first contact openings and the second contact openings further comprises:

performing a first etching operation to remove the second dielectric layer within the first openings and the second openings so that the first openings expose the buffer layer and the second openings expose the cap layers;

performing a second etching operation to remove the buffer layer within the first opening and the cap layer within the second openings so that the first openings expose the first dielectric layer and the second openings expose the gate conductive layer of the stack gate structures in the second region to form the second contact openings; and

performing a third etching operation to remove the first dielectric layer within the first openings to form the first contact openings.

[c14] 14. The method of claim 13, wherein the first etching operation, the second etching operation and the third etching operation are all carried out inside the reaction chamber of a processing station.

[c15] 15. The method of claim 14, wherein material constituting the buffer layer and the cap layer comprises silicon nitride formed using gaseous reactants CF_4, CHF_3, O_2 and Ar.

[c16] 16. The method of claim 12, wherein the first mask layer

further comprises a plurality of third openings within the second region above some of the conductive regions, and the step of removing the second dielectric layer and its underlying buffer layer and cap layer within the first openings and the first dielectric layer within the second openings comprises:
removing the second dielectric layer and its underlying first dielectric layer within the third openings to form the third contact openings.

[c17] 17. The method of claim 16, wherein the step of forming the first contact openings, the second contact openings and the third contact openings further comprises:
performing a first etching operation to remove the second dielectric layer within the first openings, the second openings and the third openings so that the first openings expose the buffer layer, the second openings expose the cap layers and the third openings expose the first dielectric layer;
performing a second etching operation to remove the buffer layer within the first opening and the cap layer within the second openings so that the first openings expose the first dielectric layer and the second openings expose the gate conductive layer of the stack gate structures in the second region to form the second contact openings; and

performing a third etching operation to remove the first dielectric layer within the first openings and the third openings to form the first contact openings and the third contact openings.

[c18] 18. The method of claim 17, wherein the first etching operation, the second etching operation and the third etching operation are all carried out within the reaction chamber of a processing station.

[c19] 19. The method of claim 18, wherein material constituting the buffer layer and the cap layers comprises silicon nitride formed using gaseous reactants CH_4, CHF_3, O_2 and Ar.